Week 14

Thin Film Transistors 2

Ambipolar and Other Transistor Architectures

Morphology

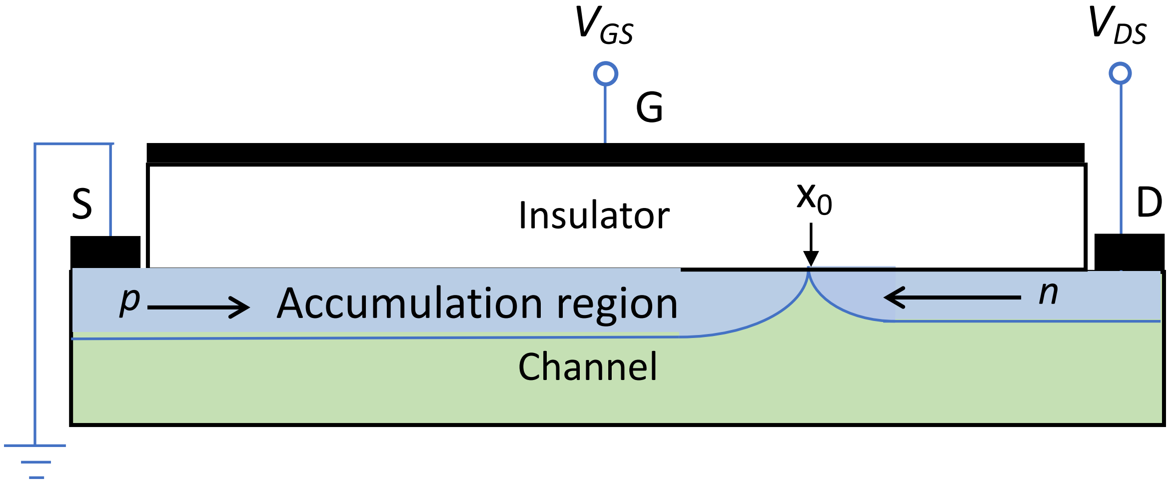
Reliability

Applications

Chapter 8.3.2-8.4, 8.6-8.9

Ambipolar OTFTs

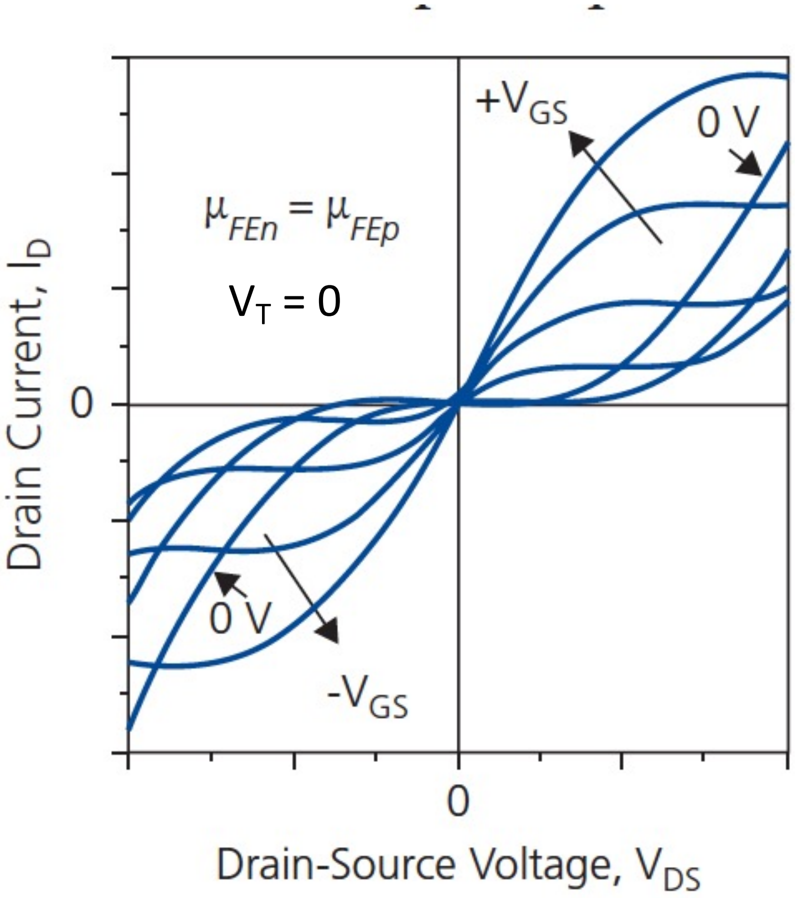
- Channel capable of supporting both electron and hole transport
- Advantage: Complementary logic possible with a single structure



Strategies for achieving bipolar action:

- Use material with both high μ_{FEn} and μ_{FEp} with contacts in the middle of the energy gap (i.e. use ambipolar conducting organics)
- Use a bilayer, one with higher electron vs. hole mobility and vice versa
- Use a blend of electron and hole transporting materials

Ambipolar transfer characteristics



Example: $V_{Tp} < V_{Tn}$

Linear regime

$$I_D = \frac{WC_i}{L}\mu_{FEn}\left(V_{GS} - V_{Tn} - \frac{V_{DS}}{2}\right)V_{DS}$$

$$\begin{pmatrix} 0 \le V_{DS} \le V_{DSsat} \\ V_{GS} > V_{Tn} \end{pmatrix}$$

Saturation regime

$$I_D = \frac{WC_i}{2L}\mu_{FEn}\left(V_{GS} - V_{Tn}\right)^2$$

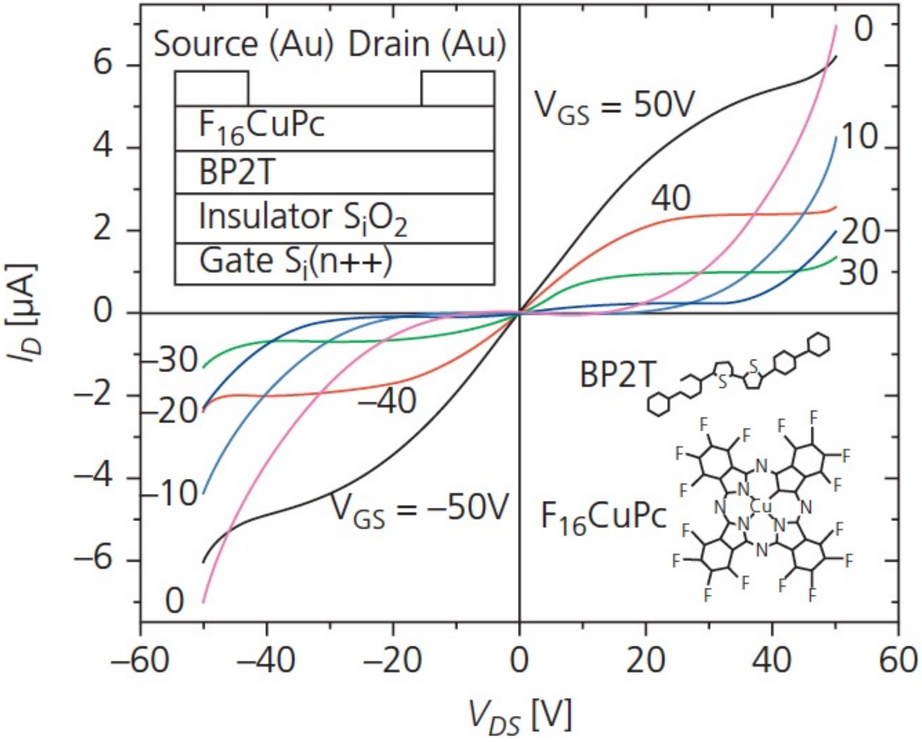
$$\begin{pmatrix} V_{DS} \ge V_{GS} - V_{Tn} \\ V_{DS} \le V_{GS} - V_{Tp} \end{pmatrix}$$

Ambipolar (quadratic) regime

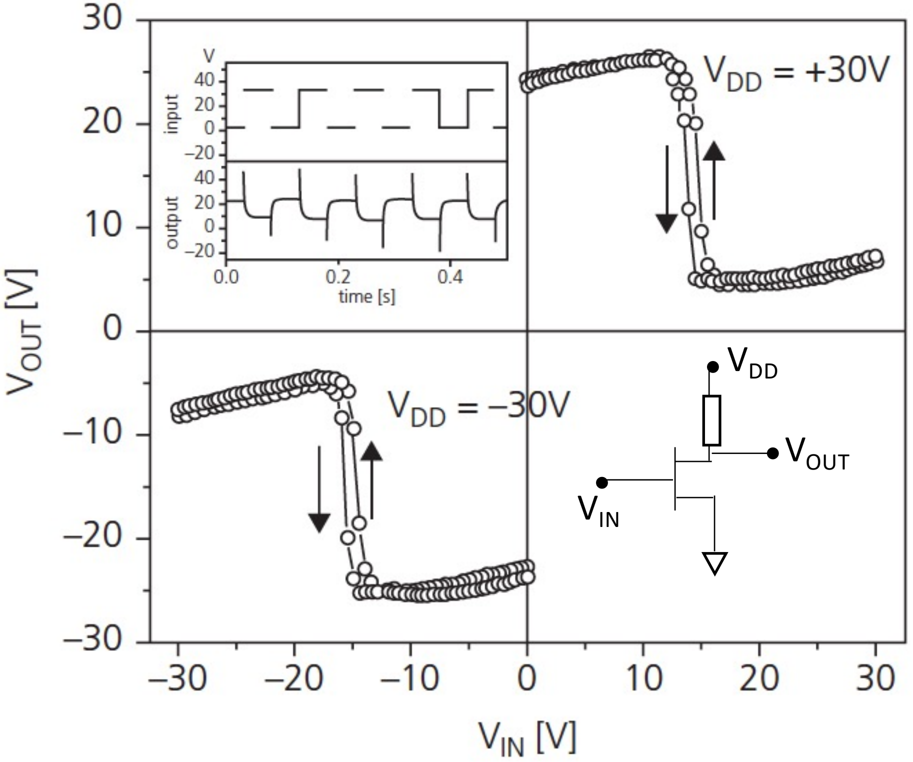
$$I_D = \frac{WC_i}{2L}\left\{\mu_{FEn}\left(V_{GS} - V_{Tn}\right)^2 + \mu_{FEp}\left(V_{DS} - V_{GS} + V_{Tp}\right)^2\right\}$$

$$V_{DS} \ge V_{GS} - V_{Tp} \ge V_{GS} - V_{Tn}$$

Bilayer ambipolar OTFT



Common source amplifier response

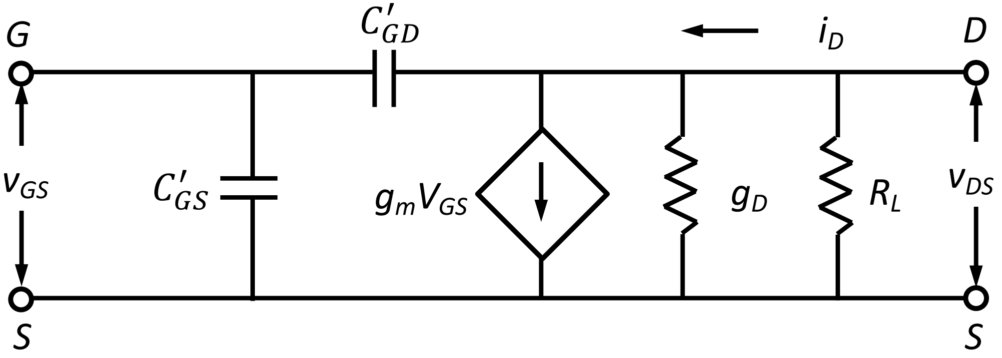


Disadvantage of the ambipolar OTFT: I_{on}/I_{off} is small since no condition where one carrier type is completely absent.

Wang et al., Appl. Phys. Lett. 88, 133508 (2006)

OTFT Bandwidth

Small signal equivalent circuit



C_{GS}'=total gate-source capacitance (including parasitics)
C_{GD}'=total gate-drain capacitance
R_L = external load resistance

Small signal input (gate) current: $i_{GS} = WLC_G \left.\frac{\partial v_{GS}}{\partial t}\right|_{V_{DS}} = j\omega\left(WLC_G\right)v_{GS} = j2\pi f\left(WLC_G\right)v_{GS}$

Small signal output (drain) current: $i_D \simeq g_m v_{GS}$

The maximum transistor bandwidth is reached when the current gain $\left|\frac{i_D}{i_G}\right| = 1$

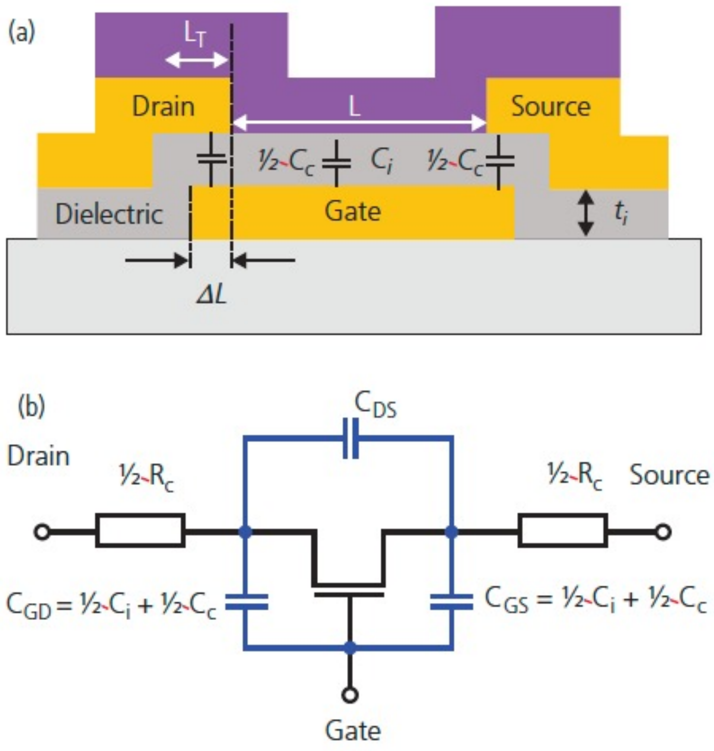
From these expressions, we get the cutoff, or transfer frequency:

$$\boxed{f_T = \frac{g_m}{2\pi WLC_G} \Rightarrow \frac{g_m}{2\pi WL\left(C_{GS} + C_M\right)}}$$

C_M = Miller capacitance

Contact Resistance Limits OTFT Performance

Sources of Parasitic Resistance and Capacitance

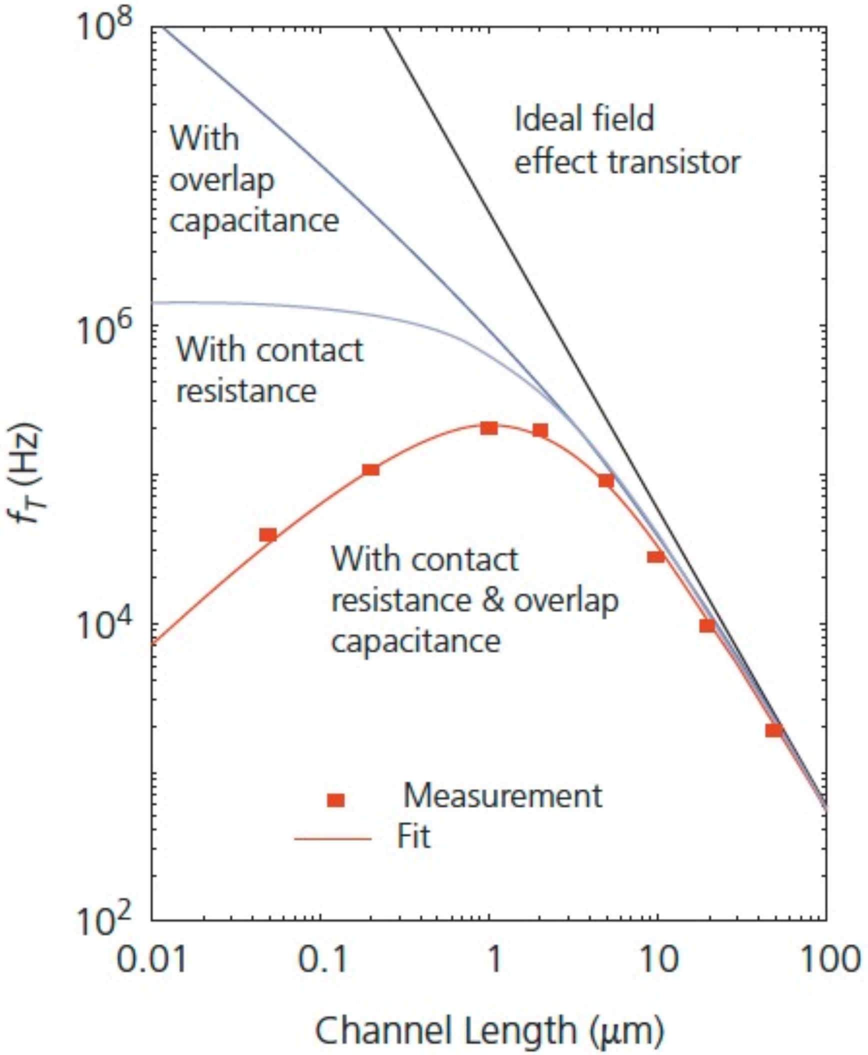


This leads to corrected transconductance and output conductance...

$$g'_m = \frac{g_m}{1 + r_S g_m} \qquad g'_D = \frac{g_D}{1 + \left(r_S + r_D\right) g_D}$$

... and frequency response

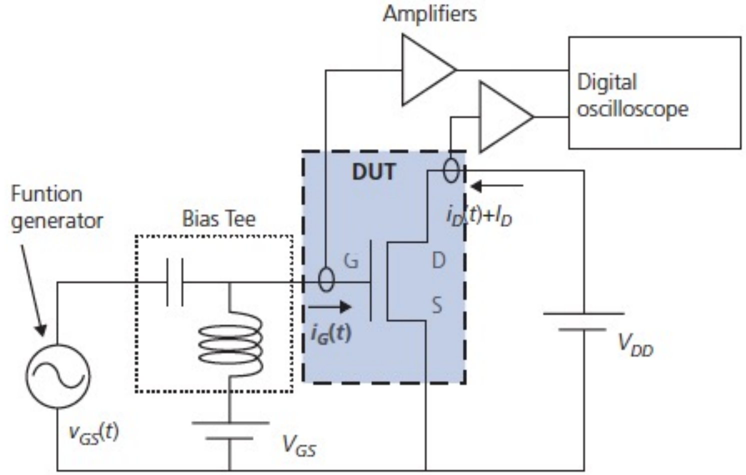
$$f_T = \frac{\mu_{FE0}\left(V_{GS} - V_T\right)}{2\pi L\left(L + \Delta L\right)}\left[\frac{1}{1 + W\mu_{FE0} C_G \left(V_{GS} - V_T\right) R_C / L}\right]$$



Hoppe, et al., Organic Electron., 11, 626 (2010)

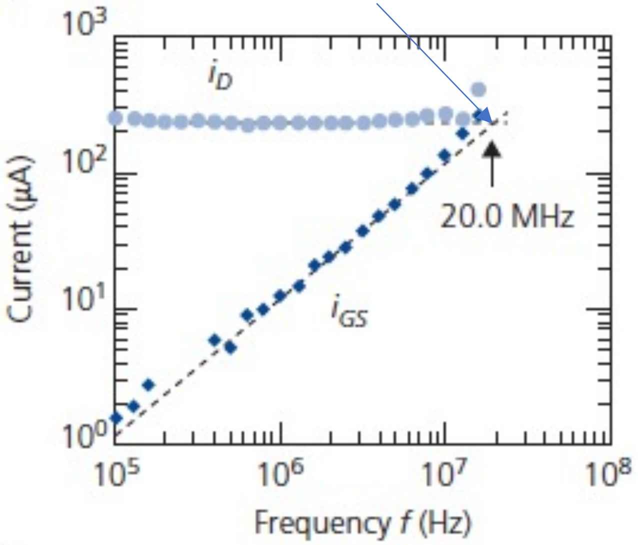
$$R_C = r_S + r_D$$

Example: High Bandwidth OTFT

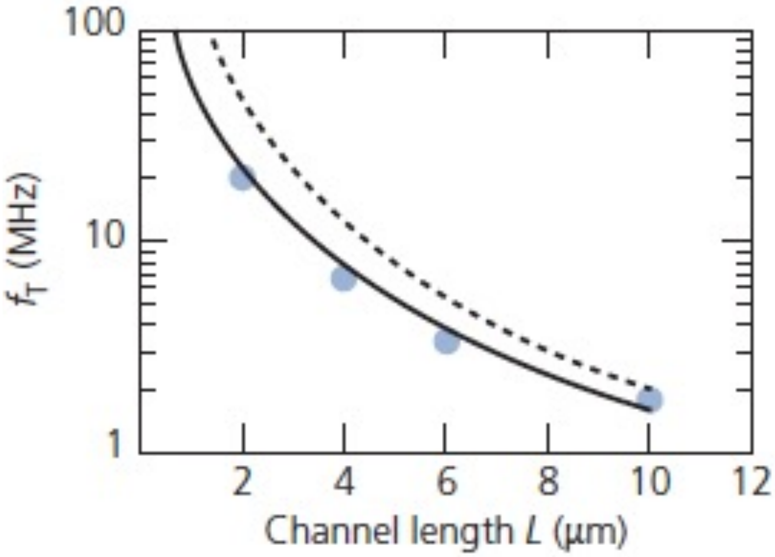


Frequency test circuit

Current gain = 1



C$_{60}$ n-channel OTFT



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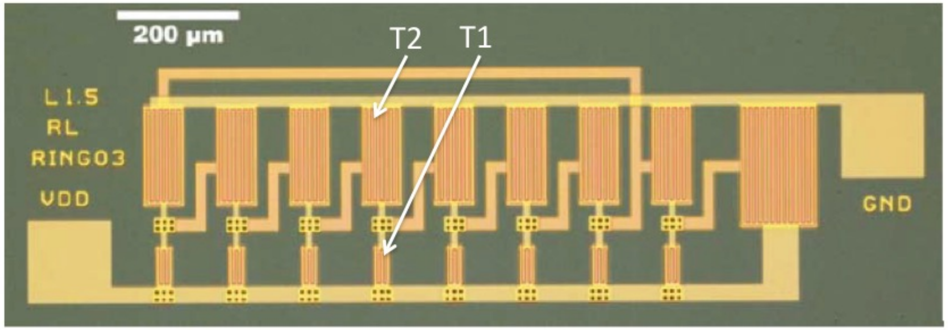
est

Kitamura & Arakawa 2009. *Appl. Phys. Lett.,* 95**,** 023503.

Performance has come a long way

7 stage ring oscillator

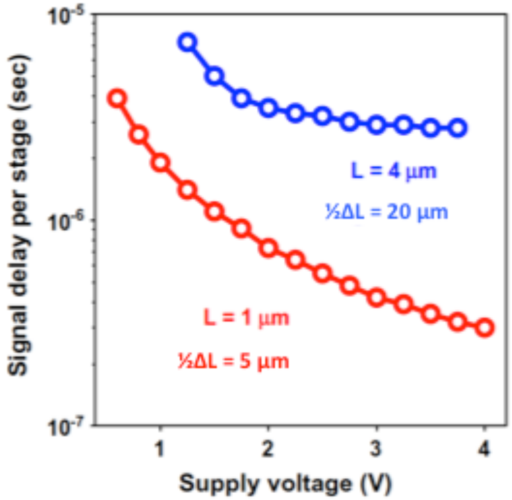


Smith et al., Appl. Phys. Lett., 93, 253301 (2008)

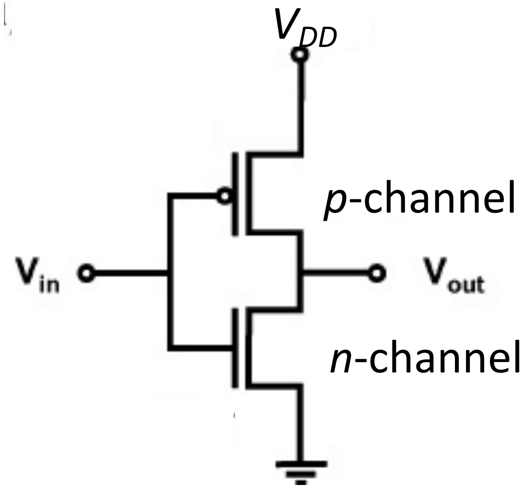
Oscillation frequency a function of the delay per gate

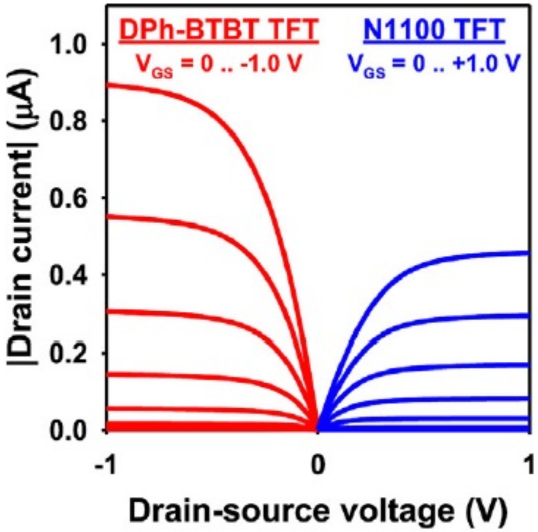
$$2f_{osc} = 1/N\tau_{delay}$$

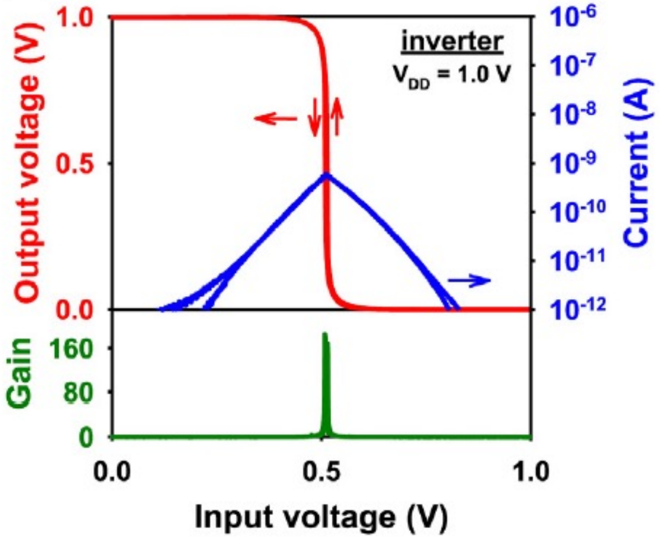
$$f_{delay} = \left(2\tau_{delay}\right)^{-1} < f_T$$



Zschieschang, et al., 2013. *Organic Electronics,* 14**,** 1516.



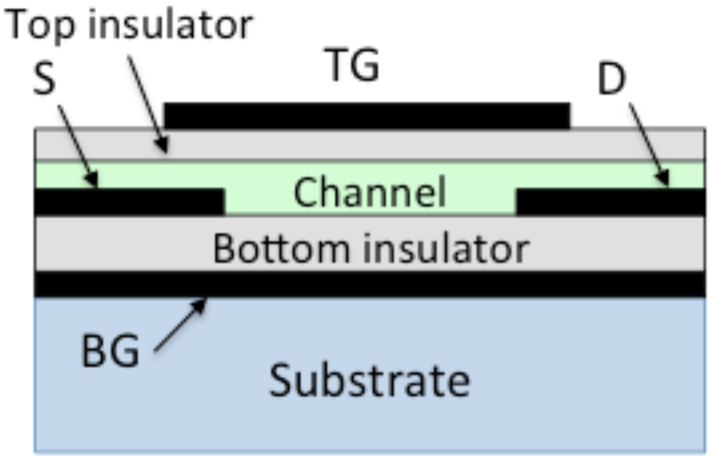




Zschieschang, et al., 2017. *Organic Electronics,* 49**,** 179.

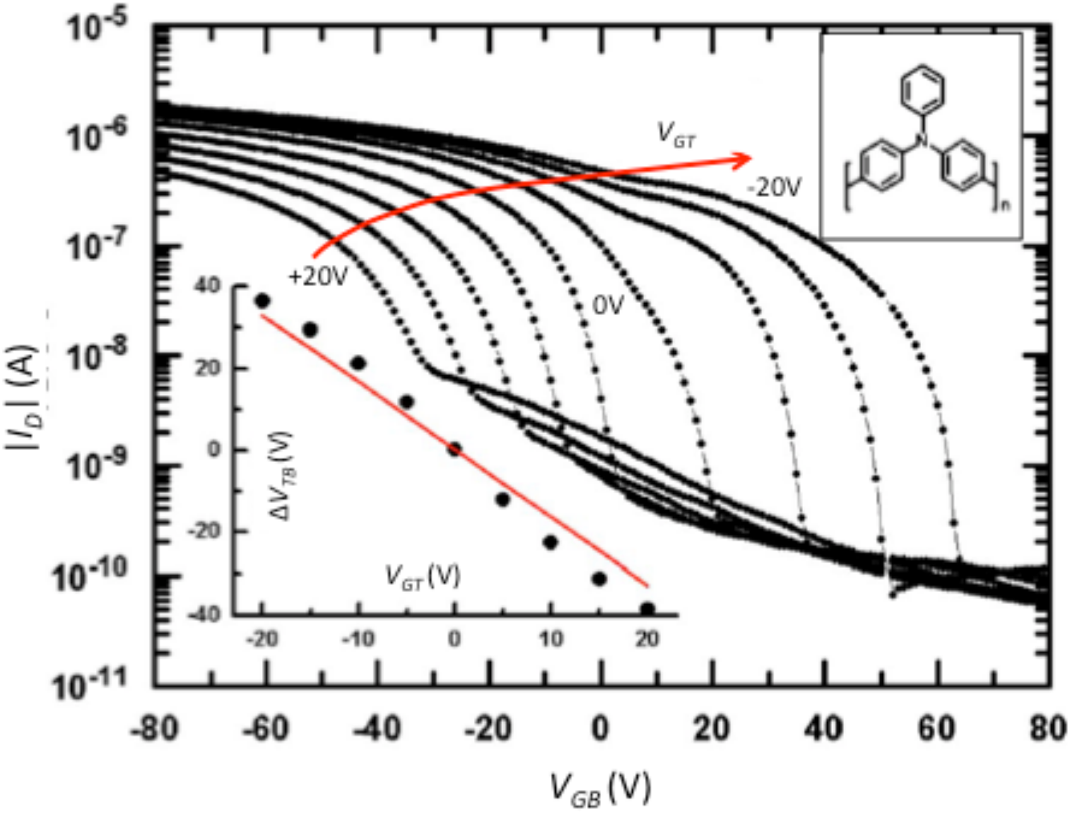
Dual gate transistors

- Useful for adjusting V_T due to extra bias control of the second (bottom) gate
- In conventional CMOS technology, this is the "body potential"
- Important for controlling large ICs



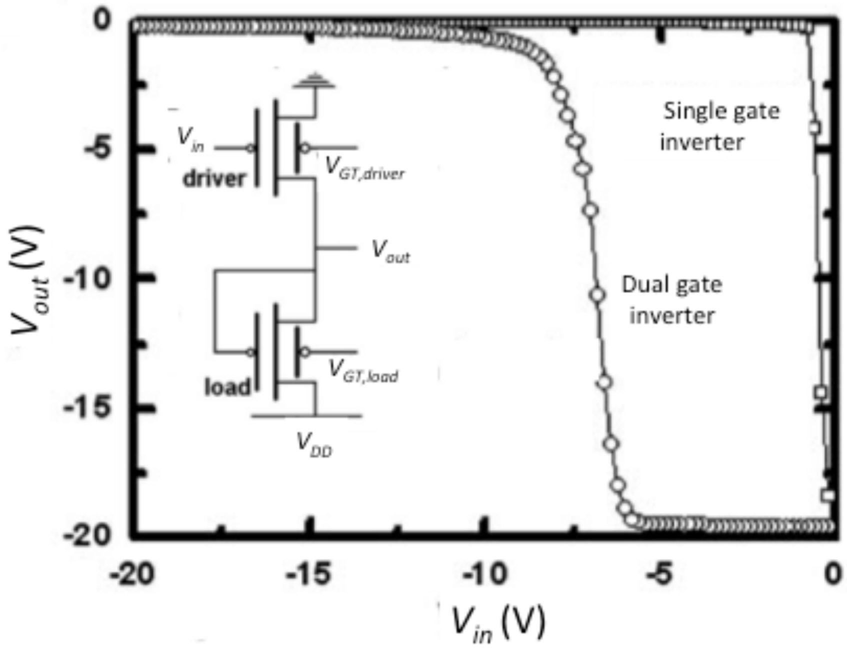
Shift in top gate threshold related to bottom gate voltage:

$$\Delta V_{TT} = \frac{C_B}{C_T} V_{GB}$$



Spijkman et al. Appl. Phys. Lett., 92 143304 (2008)

Dual gate control

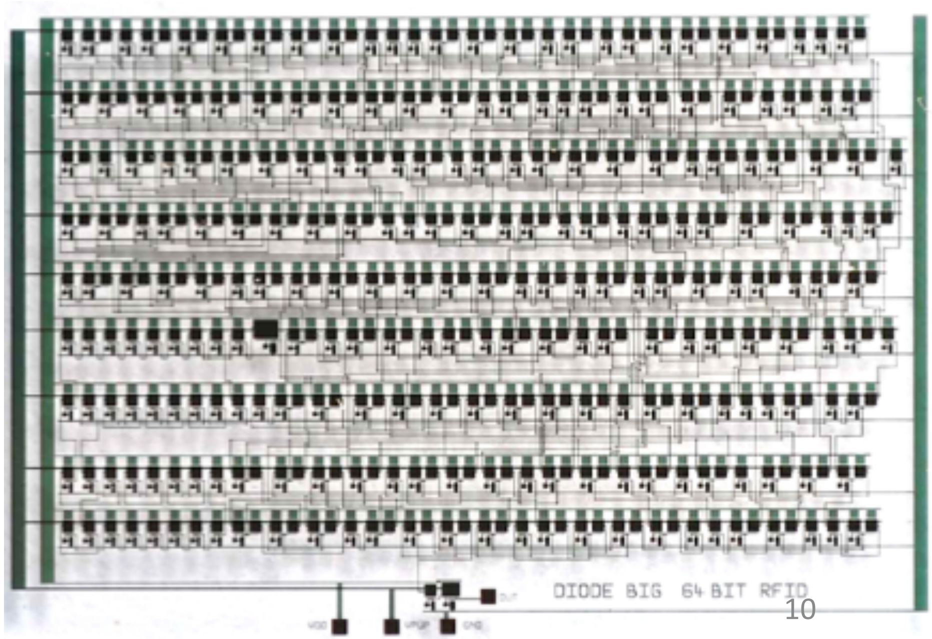


Improved noise margin
Control of circuit gain

Spijkman et al. Appl. Phys. Lett., 92 143304 (2008)

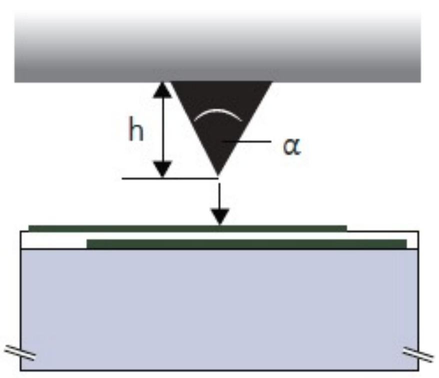
Photograph of a 64-bit RFID transponder operating at 4.3 kb/s using dual gate inverter logic.

Myny et al. IEEE J. Sol. State Circuits, 46, 1223 (2011)

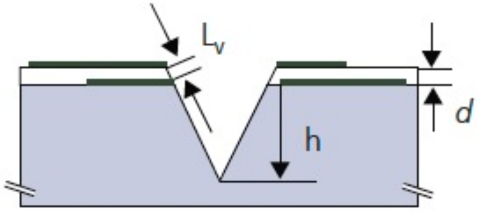


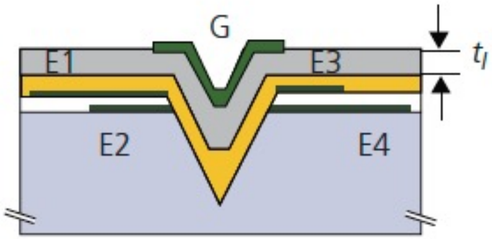
Other Device Types

V-gate transistor



Knife edge cuts through contact layers





Channel and gate insulator deposited

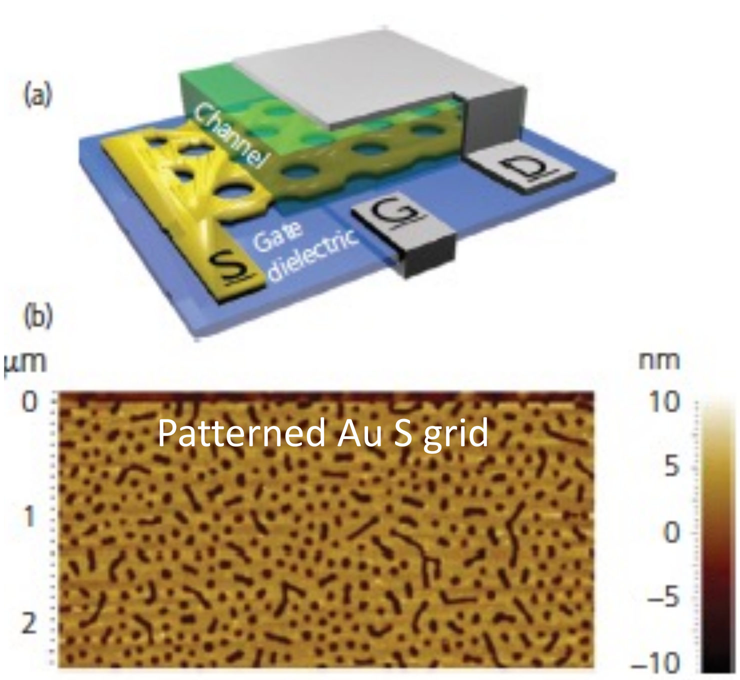
Vertical geometries reduce channel transit times ⇒ higher bandwidth
Can be more compact than lateral OTFTs
Can run in vertical mode (S=E_1, D=E_2) or horizontal mode (S=E_1, D=E_3)

Stutzman, et al., Science, 299, 1881 (2003)

Other Device Types

Permeable gate transistor

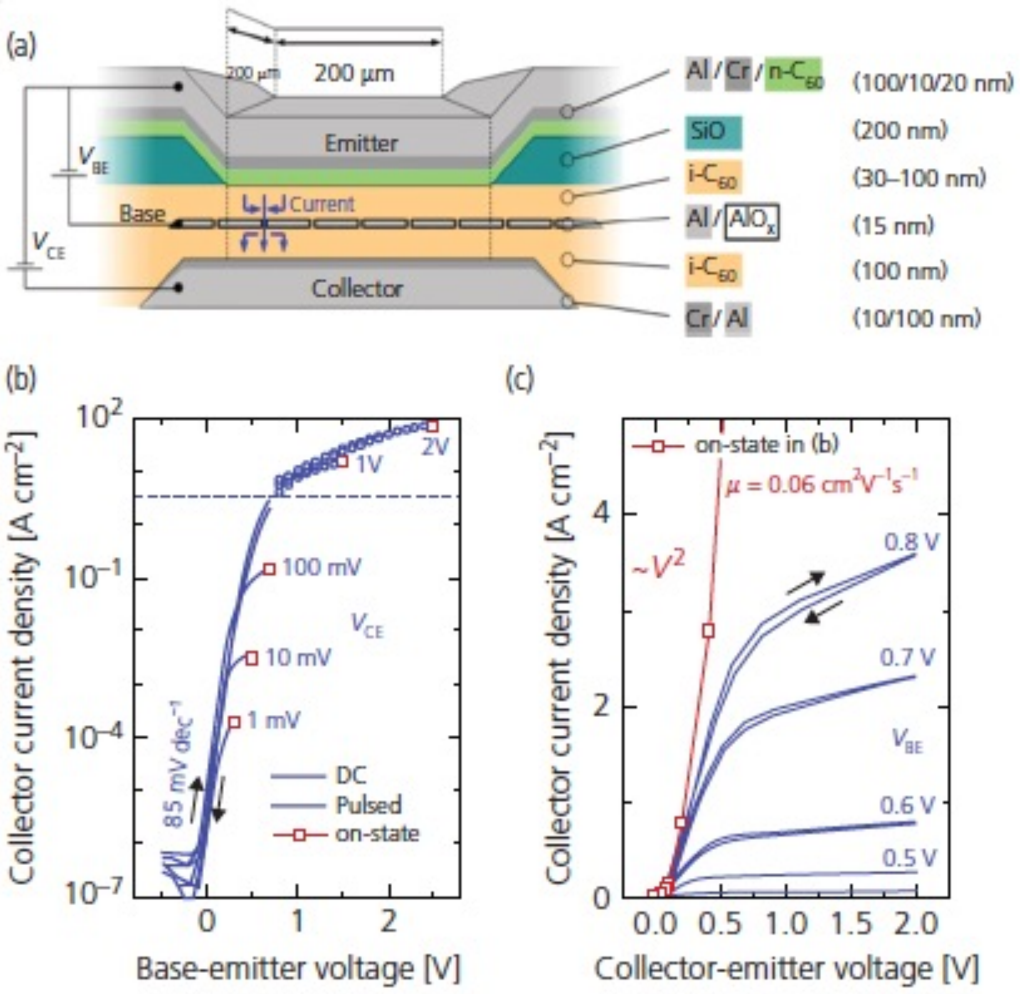
Permeable source V-FET



Gate (removed from S by gate dielectric) controls S-D current by attraction or repulsion of charge

Ben-Sasson et al., (2009). Appl. Phys. Lett., 95, 302.

Permeable Base transistor

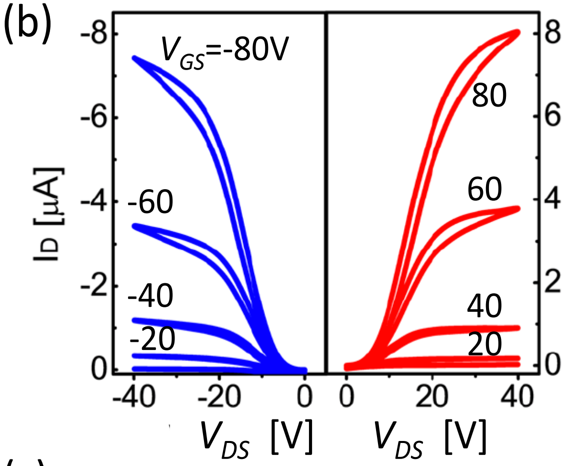


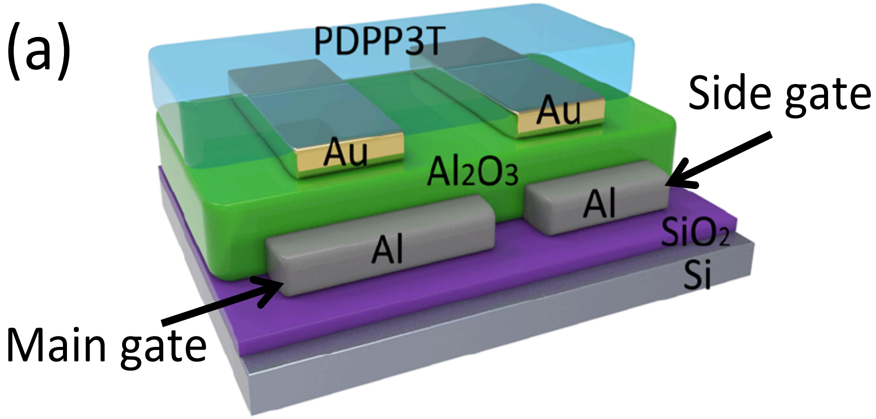
Klinger et al. (2017). Scientific Reports, 7, 44713.

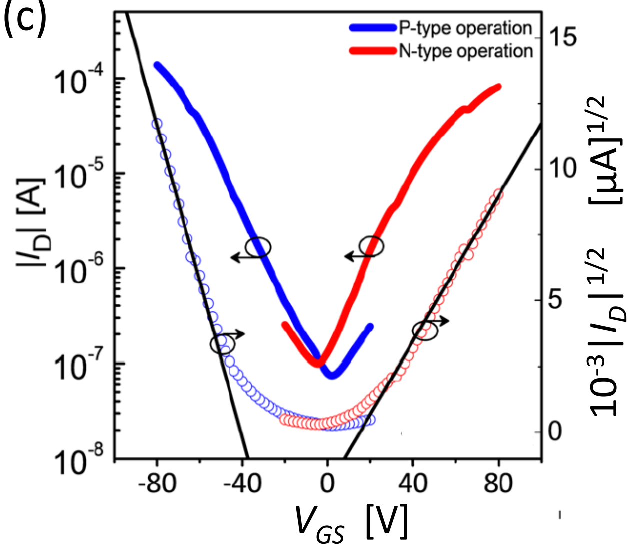
Other Device Types

Split gate transistor

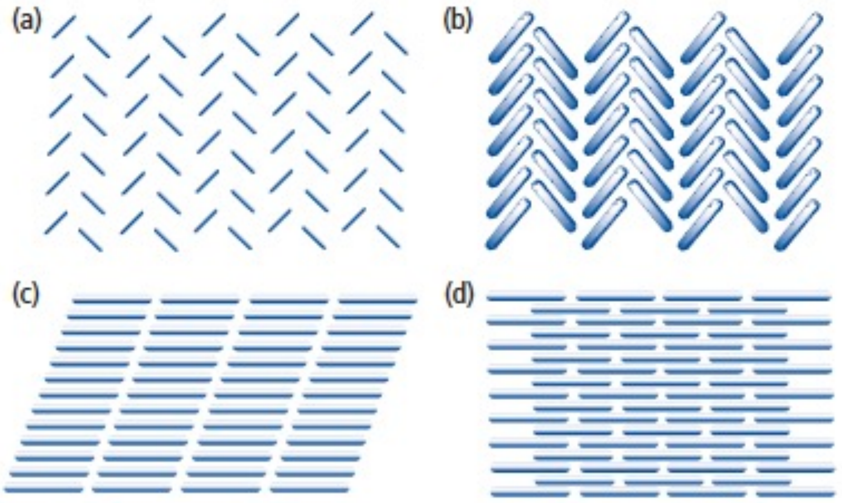
- When gates shorted: ambipolar
- Otherwise, operated as p or n-channel



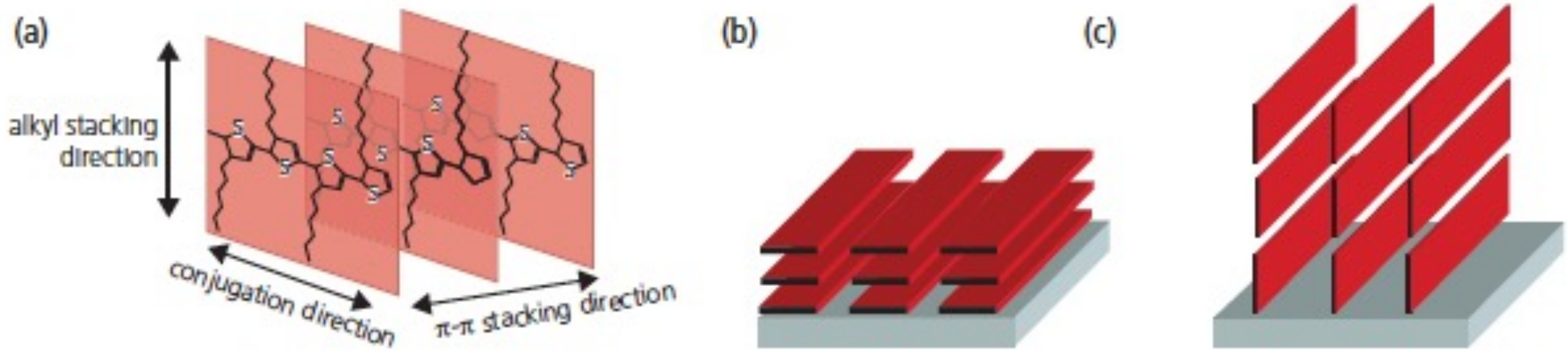




Highest mobilities when π-stacking is in the transistor plane



Different, common organic stacking motifs
(see Chapter 2)

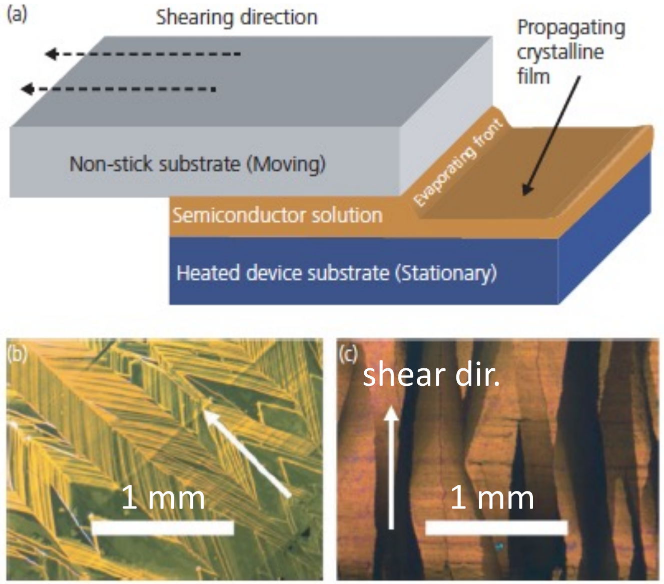


best vertical conduction

best in-plane conduction

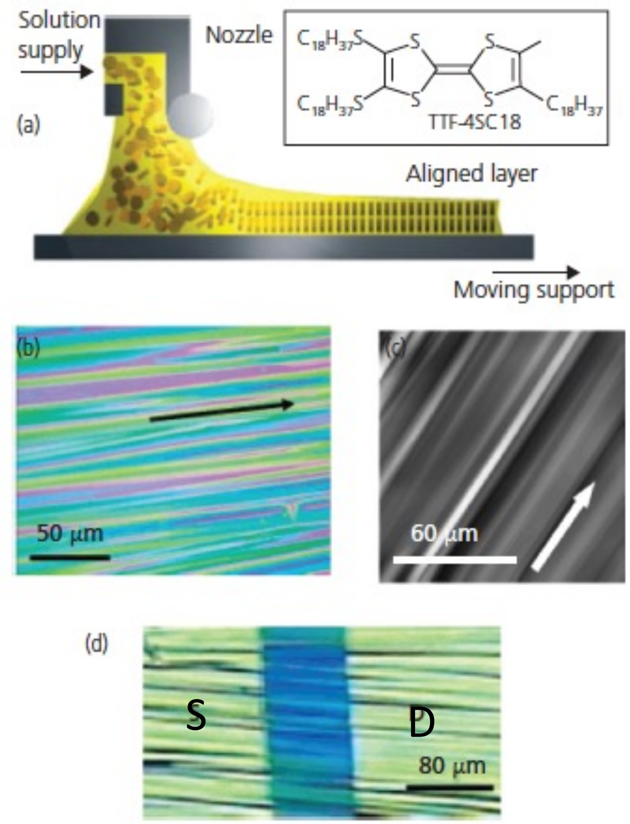
Methods for Orienting the Channel Semiconductor

solution shearing



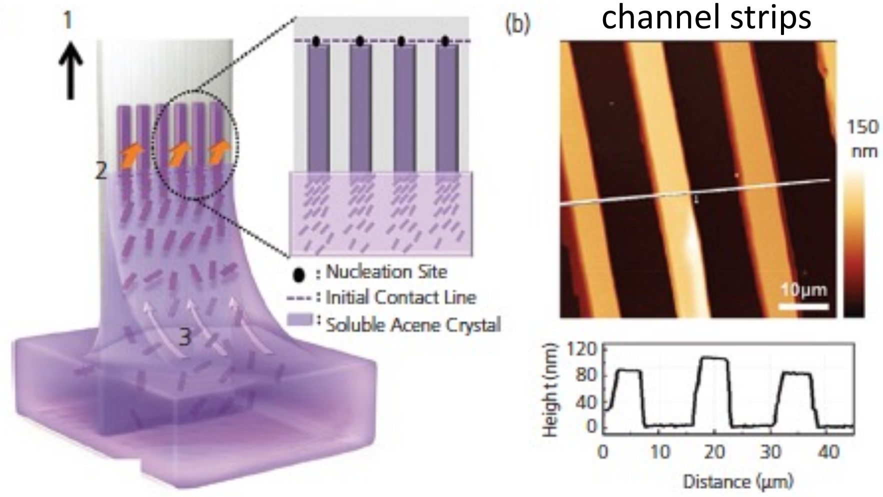
Liu, et al., Z. (2009) Adv. Materials, 21, 1217

zone casting



Miskiewicz, et al. (2006). Chem. Materials, 18, 4724.

dip coating

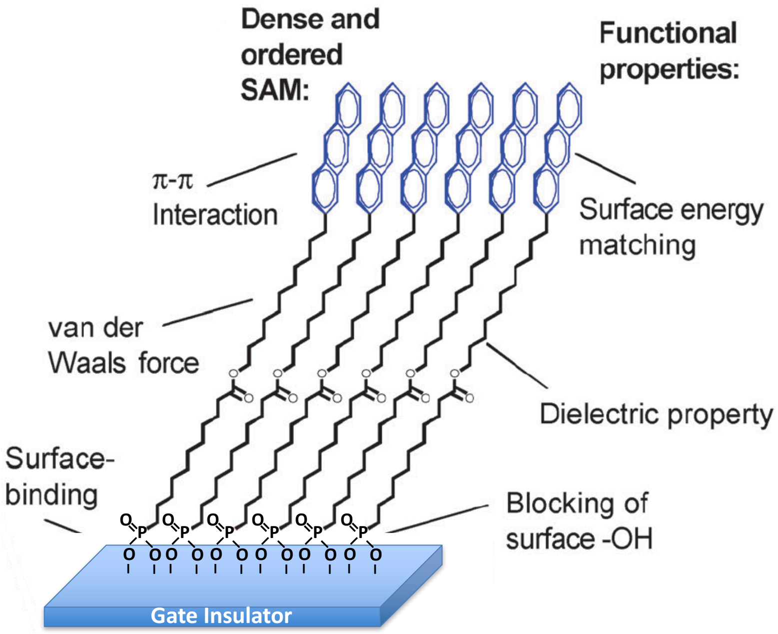


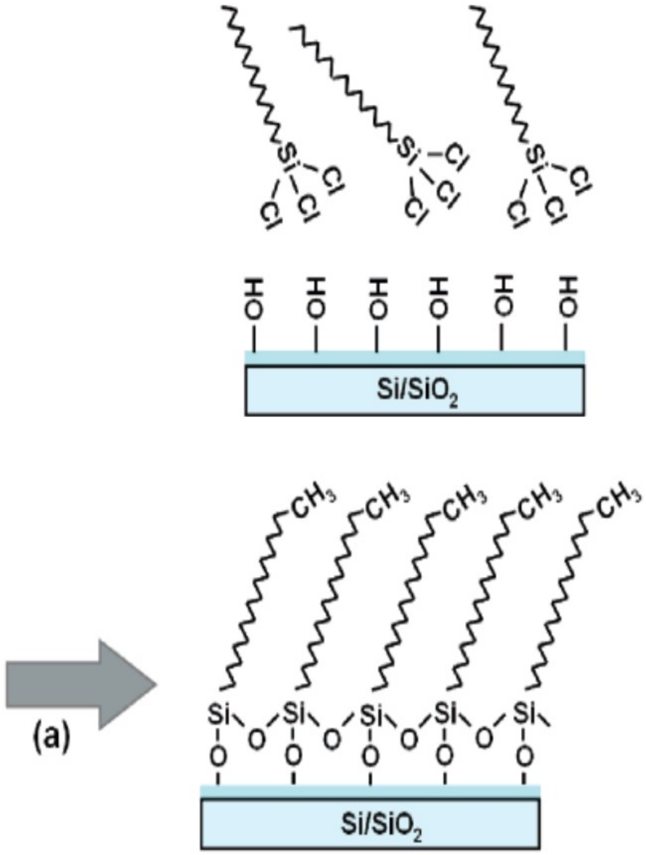
TIPS-pentacene channel strips

Jang et al., (2012) Adv. Functional Materials, 22, 1005

Achieving Optimal Morphologies

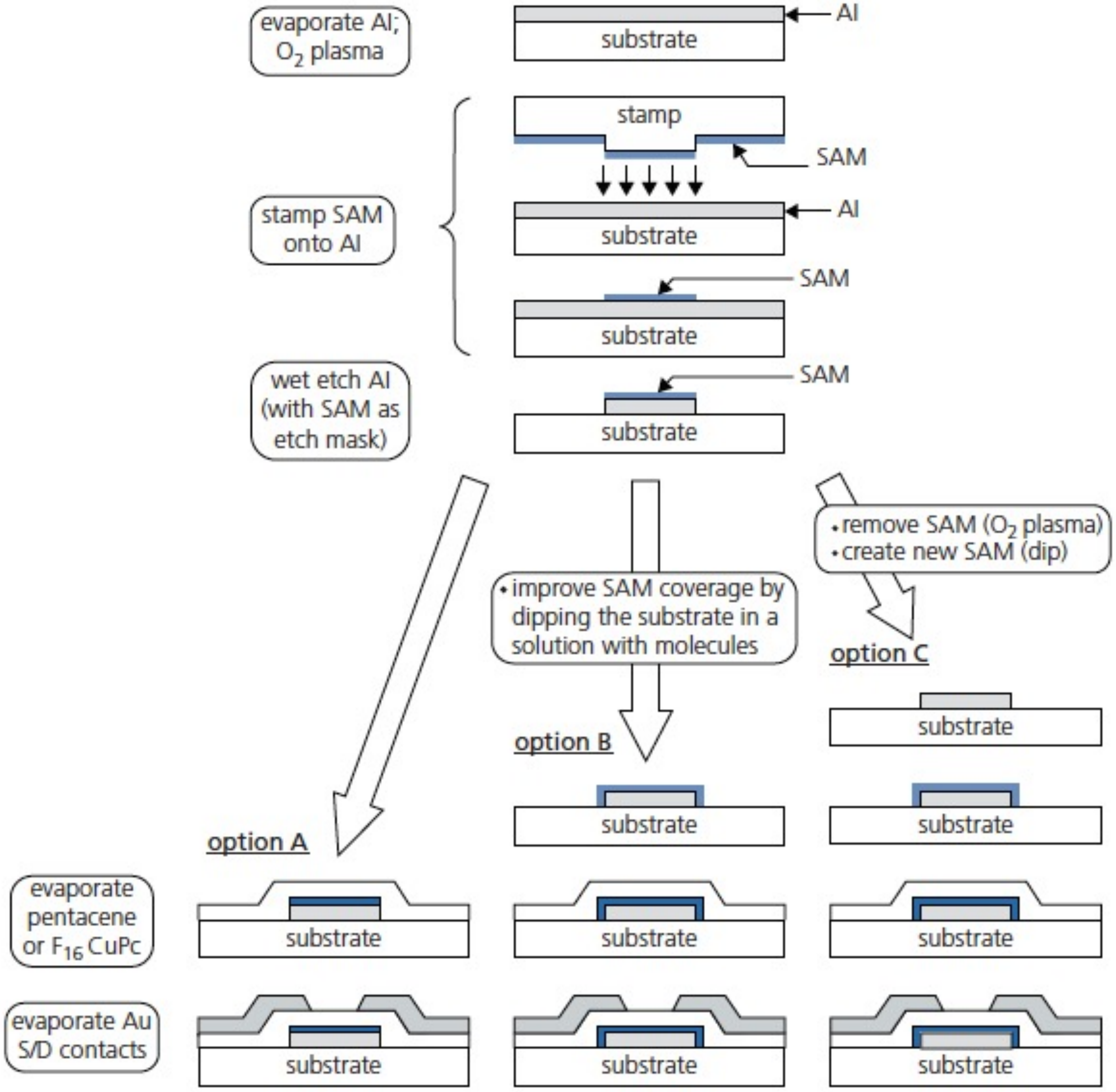
- Method 1: Control during growth by VTE, OVPD, solution
- Method 2: Use Self Assembled Monolayer (SAM) functionalization to initiate growth of desired structures by vapor or solution deposition

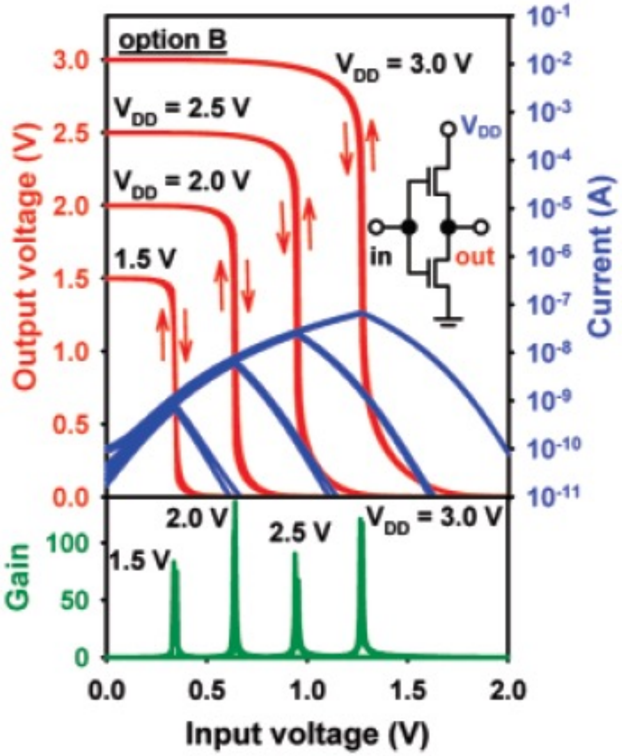




Example: Octyltrichlorosilane (OTS)

Contact Printing Initiated by SAM



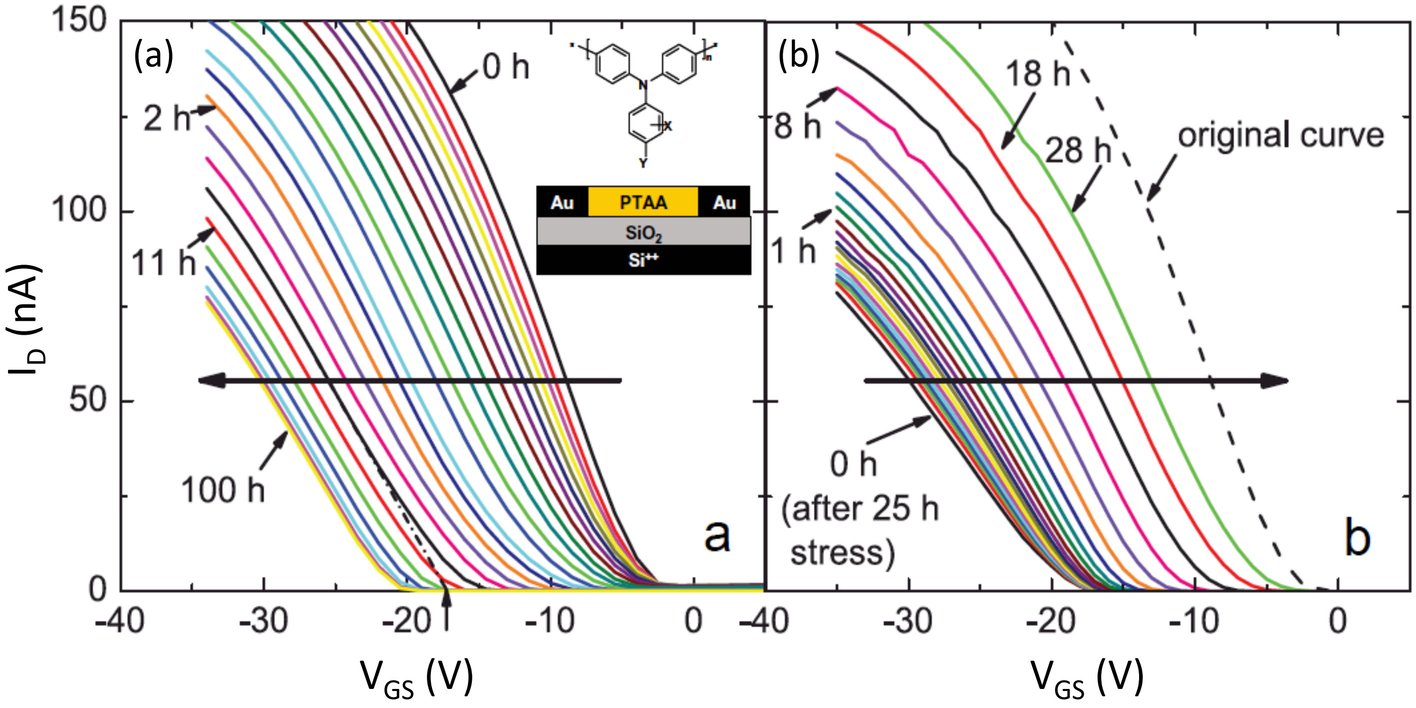


Pentacene (p)
F_{16}CuPc (n)

Zschieschang, et al., 2008. *Langmuir,* 24 1665.

Reliability

- Threshold voltage drift the primary source of circuit failure
  - Decreasing noise margin
  - Increasing leakage



Drift $\left\{ \begin{array}{l} V_{DS} = -3V \\ V_{GS} = -20V \end{array} \right.$

Recovery

Original transfer characteristics (and V_T) partially recovered following stress

Sharma, et al. Phys. Rev. B, 82 075322 (2010).

Threshold voltage drift over time

(see Ch. 6.7 & 7.8)

- Drift due to charges migrating in insulator or channel toward the interface
  - Surface traps at the channel
  - Traps within the semiconductor bulk
  - Charge (ions) drifting within the insulator

$$\Delta V_T(t) = \Delta V_T(\infty)\left(1 - \exp\left(-\frac{t}{\tau}\right)^m\right)$$

Empirical voltage drift expression:
Stretched exponential

$m = T/T_0$ for exponential trap distribution given by:

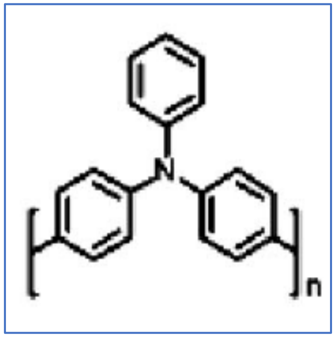
$$h_{tr}(E) = h_{tr0}\exp\left(-E/E_T\right)$$

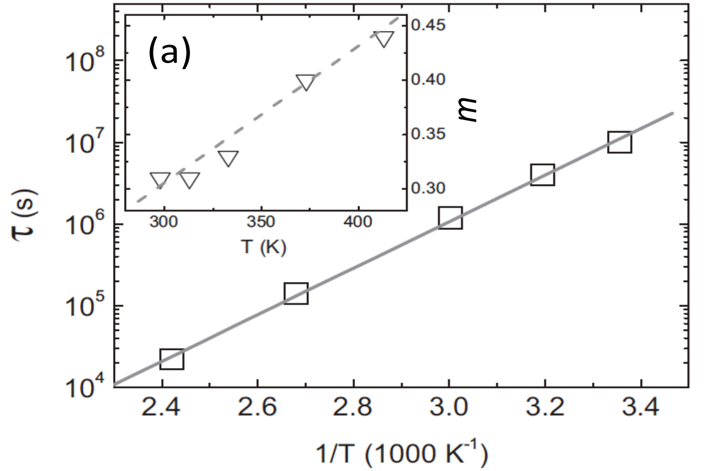
⇒ Time constant for drift

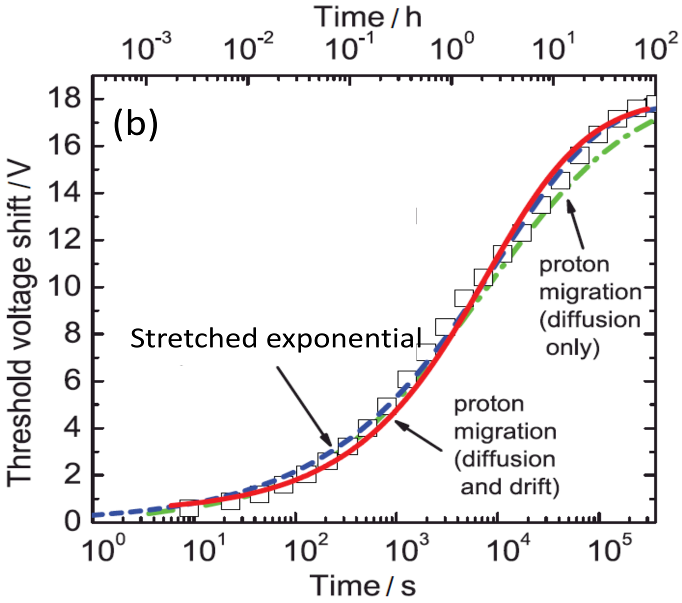
$$\tau = (2\pi\nu)^{-1}\exp\left(E_T/k_B T\right)$$

Drift occurs over an extended time, and is thermally activated

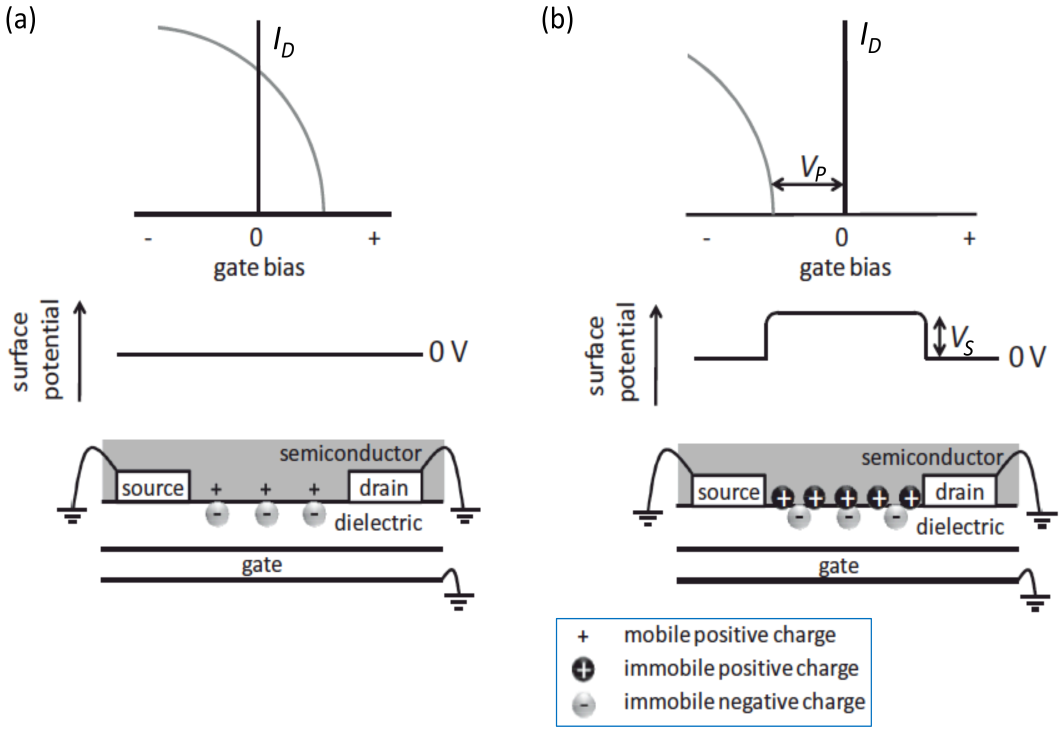
Example: Poly(triarylamine)







Bobbert et al, Adv. Mater. 24, 1146 (2012)

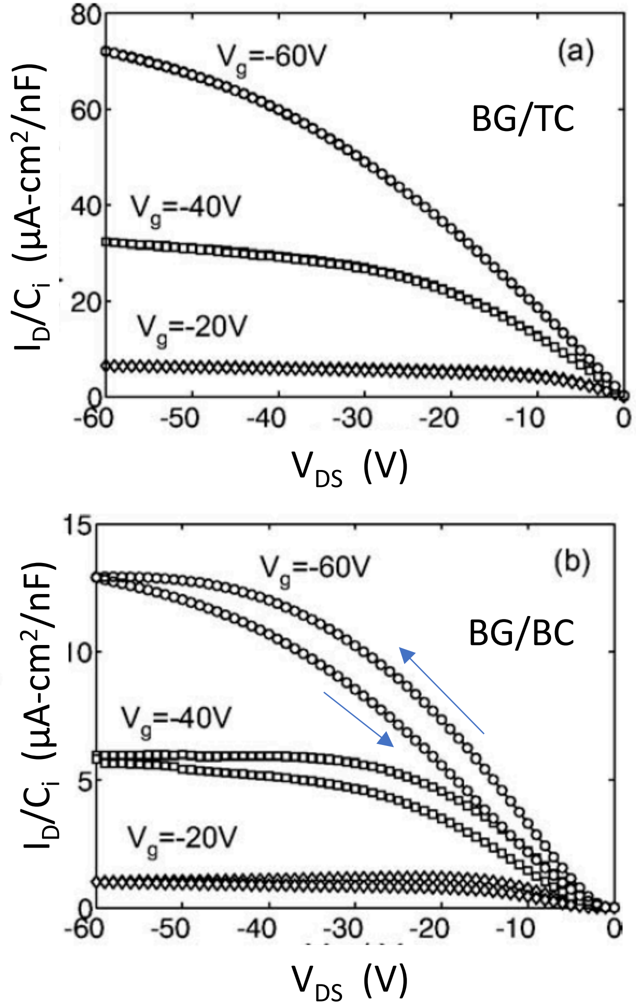


Water is the main problem: Proton generation

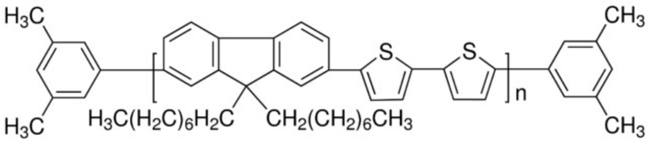
$$2H_2O \leftrightarrow 4H^+ + O_2 + 4e^-$$

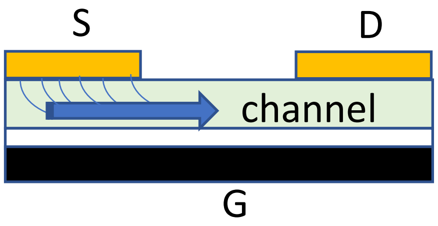
Mathijessen et al., Adv. Mater. 22, 5105 (2010)

Hysteresis: Another failure mode

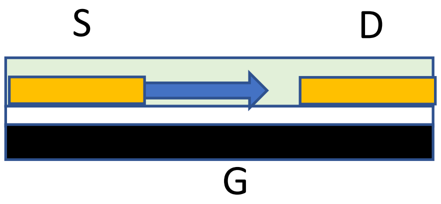


p-channel F8T2 transistors





BG/TC: Large contact area to channel
Current drawn from contact surface (arrow)



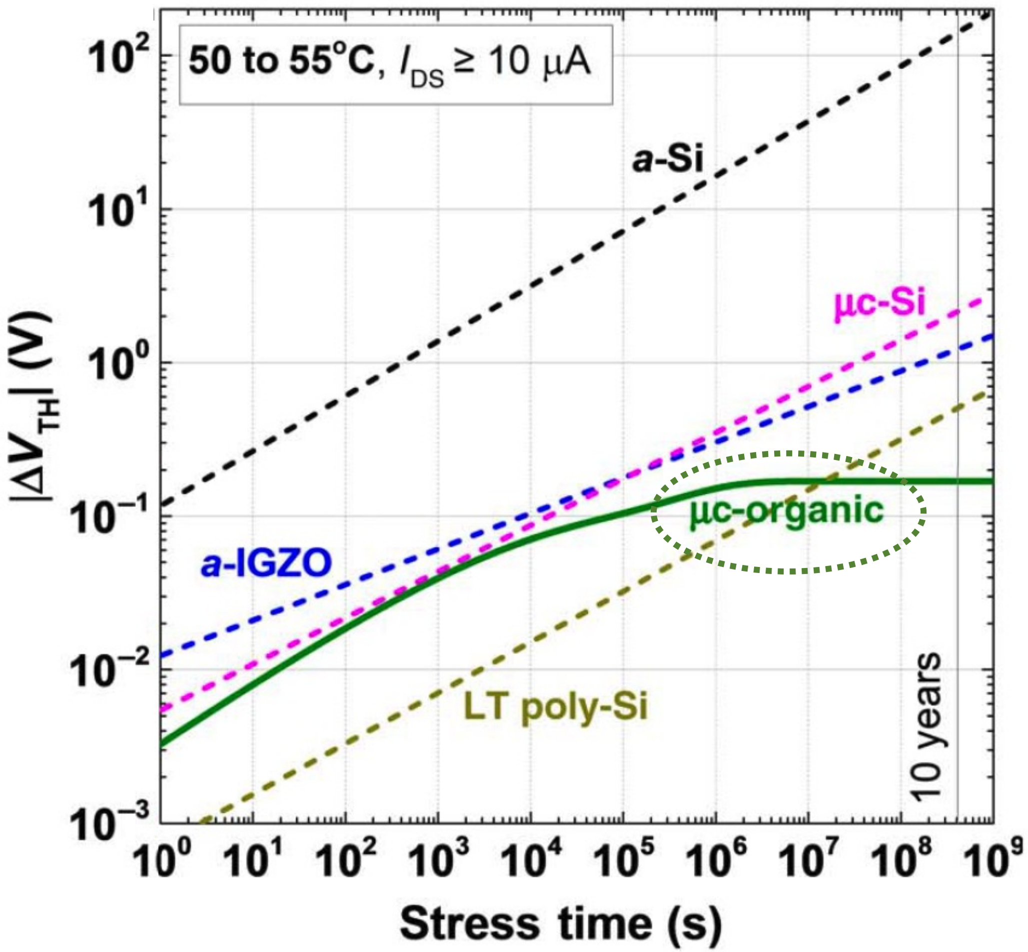
BG/BC: Small (edge) contact to channel
Current drawn from contact edge (arrow)

Drain contact trapping

Contact only via edge of the electrodes increases the current density, resulting in defect formation and charge trapping. This induces changes in V_T and I_{DS}, depending on sweep direction (arrows)

Richards & Sirringhaus Appl. Phys. Lett., 92, 023512 (2008)

Comparison of TFT Reliabilities



Jia, et al. Science Adv. 4, eaao1705, (2018)

Caveats (and there are many):

- Devices from different labs may be based on different standards and conditions
- Device selection not necessarily based on same characteristics
- Performance can vary over a wide range in any technology

Applications must exploit advantages, and cannot be vulnerable to disadvantages

To review….

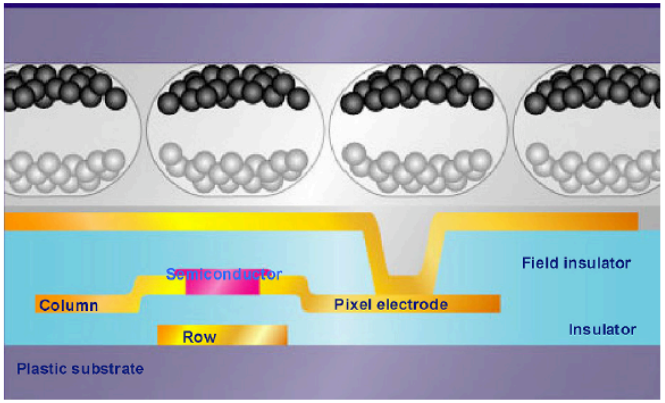
- PROs
  - ➢ Flexible, conformable, ultralight
  - ➢ Can be made over very large areas
  - ➢ Suitable for large scale R2R manufacture
- CONs
  - ➢ Cannot source large currents
  - ➢ Characteristics drift over long periods in operation
  - ➢ Limited bandwidth (≤ 1 MHz in many cases)

Voltage driven display backplanes

- Electrophoretic displays

(a)

(b)

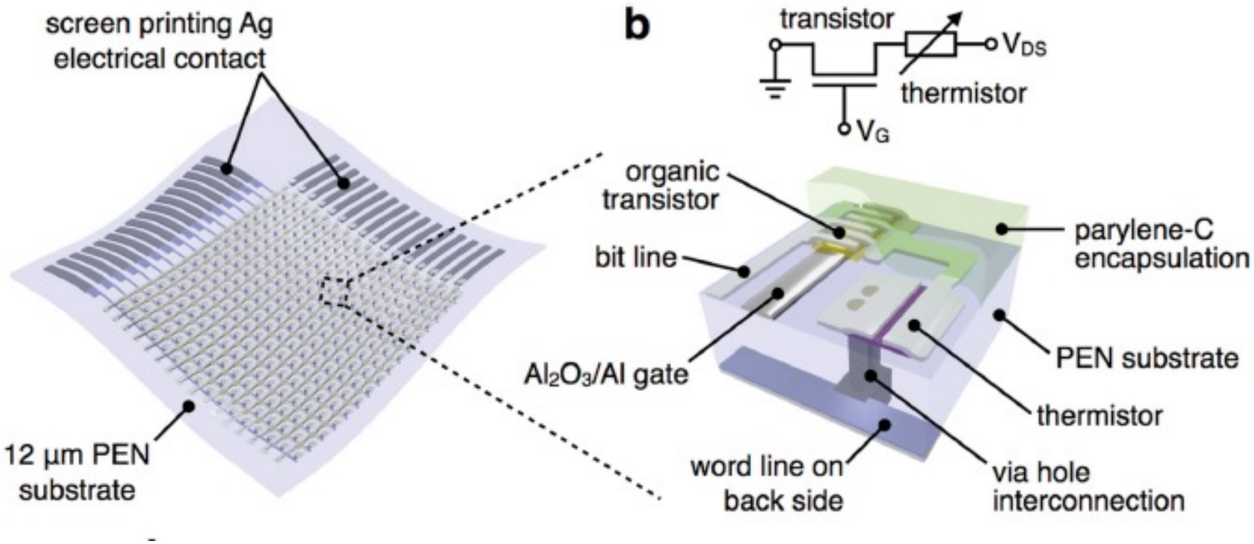


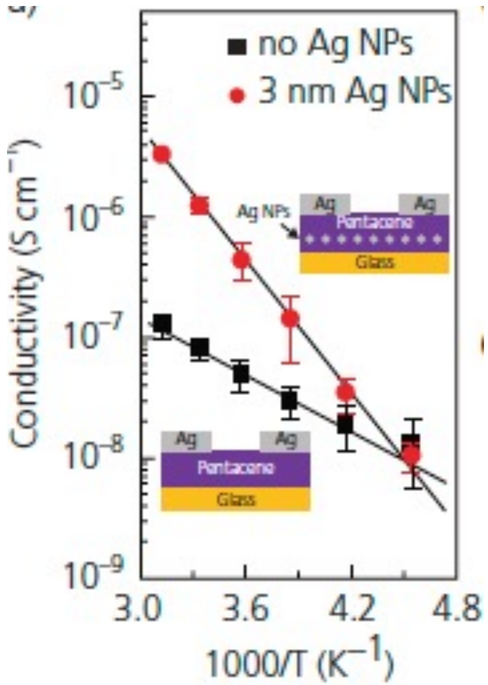
320 x 240 QVGA display
Display pixels are voltage (not current) driven

QVGA=quarter video graphics array

G. Gelinck *et al J. Soc. Info. Display,* **14**,113, 2006.

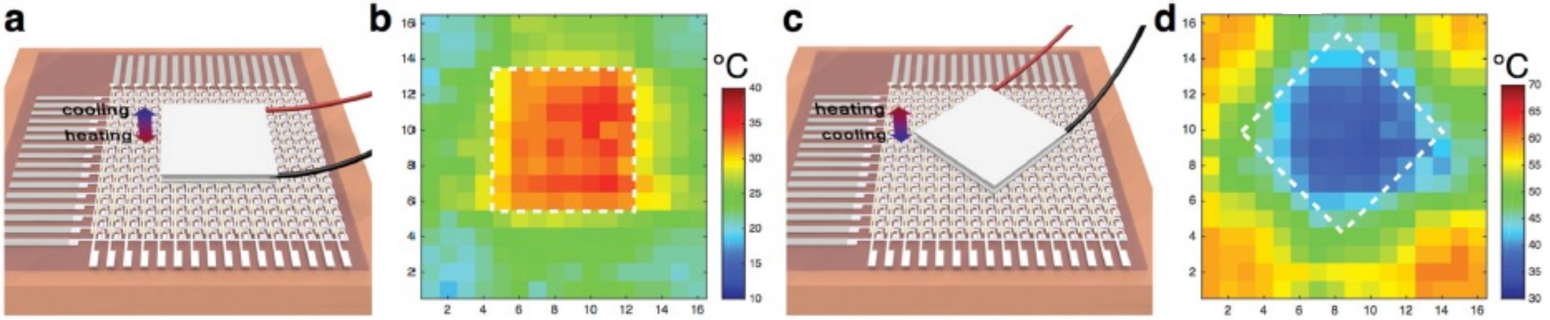
Thermal Position Sensing





Array used for detecting position of thermal source

Sensing element: channel resistance with a Ag NP layer



Ren, et al., Adv. Mater. 28, 4832 (2016)

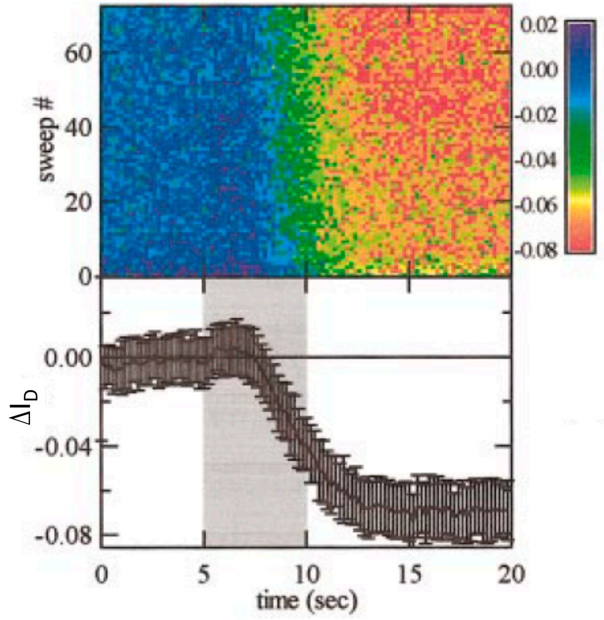
Chemical sensing

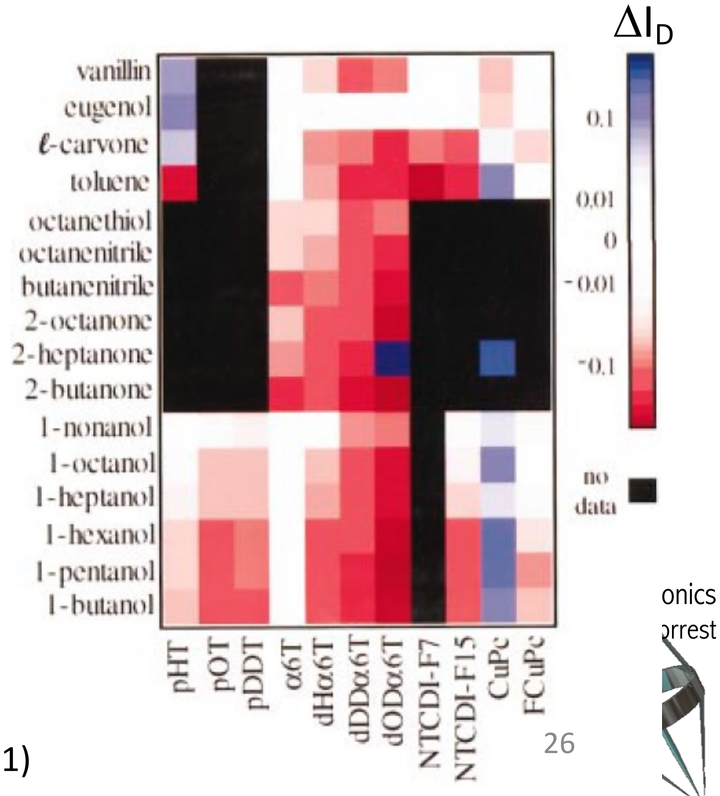
- OTFTs have demonstrated voltage drifts due to water.
- Are there other analytes that can be sensed?
- Sensor attributes
  - Fast
  - Sensitive to small doses
  - Reversible
  - Specific

16 analytes
11 transistor channel mater.

α–6T transistor

Analyte: 1-hexanol
Exposure: 5 s
Recovery: 1 min

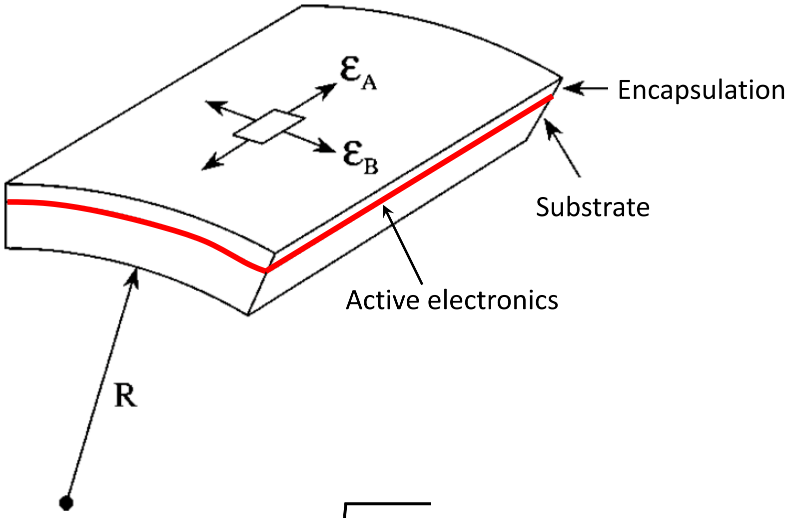




B. Crone *et al.*, 78, 2229, (2001)

Bendable Electronics

Placing active electronics at the neutral strain point
⇒ minimal stress to circuits on bending even over sharp angles

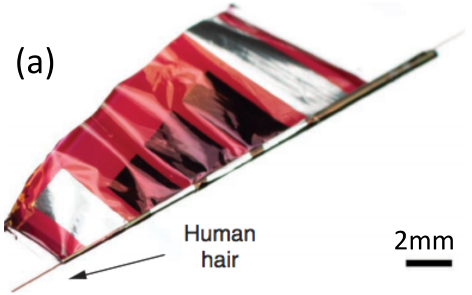


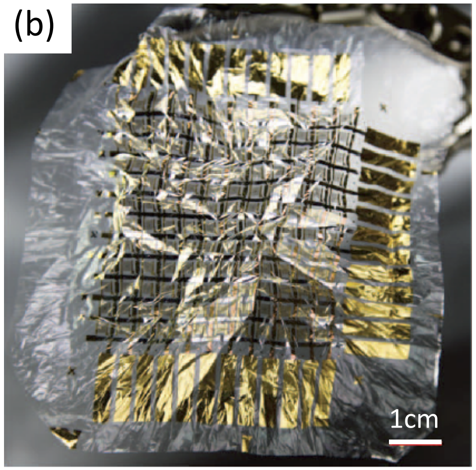
Neutral strain: $$\frac{d_{sub}}{d_e} = \sqrt{\frac{Y_e}{Y_{sub}}}$$

Y = Young's modulus (measure of material stiffness)

$$Y = \frac{FL_0}{A\Delta L}$$

F = force to extend solid
L_0 = original length
ΔL = length change
A = cross sectional area perpendicular to F

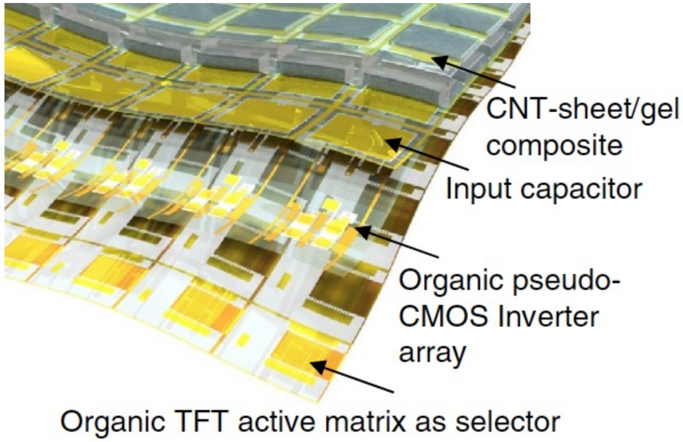


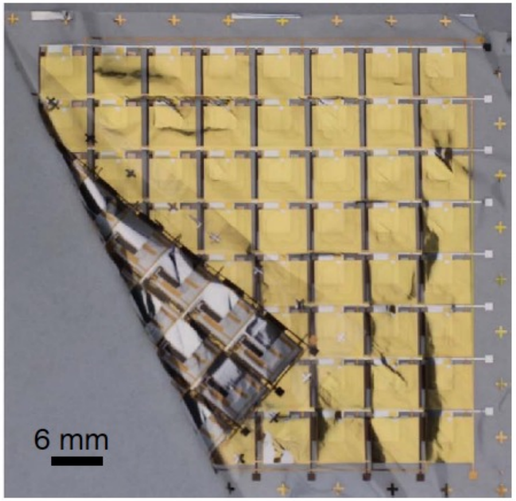


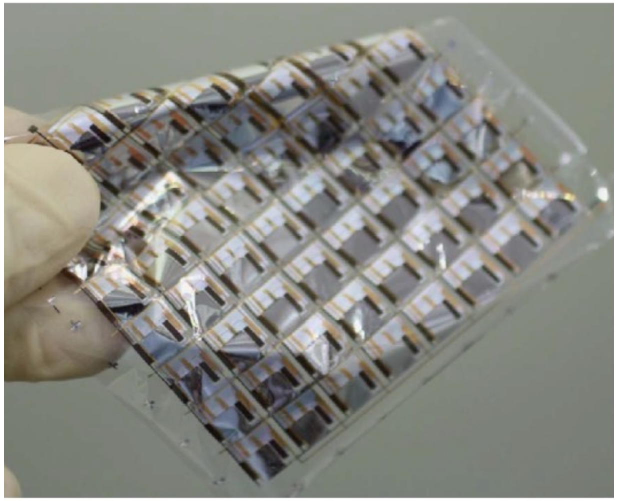
12x12 array of tactile pixels

Kaltenbrunner et al. Nat. Commun.3, 770 (2012); Nature 499, 458 (2013)

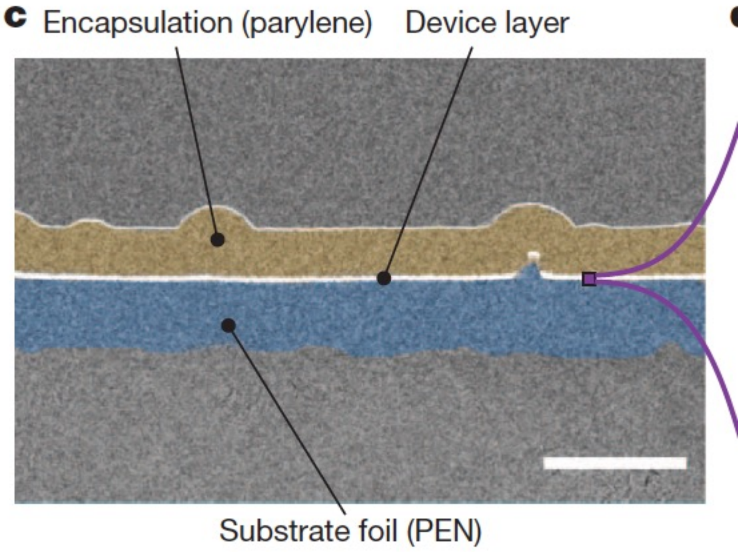
“Imperceptible” Electronics

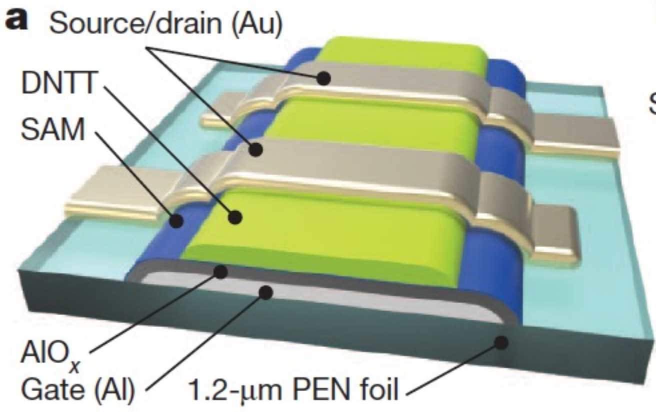






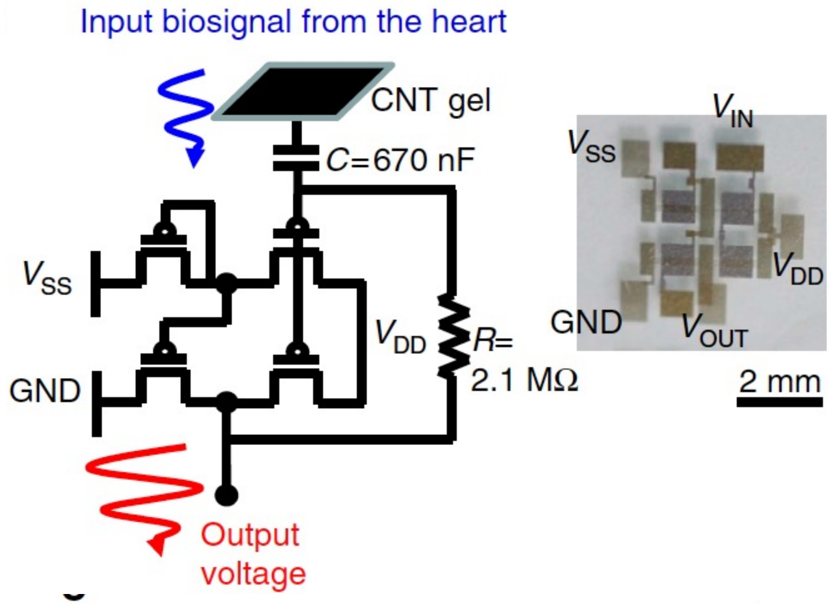
Substrates are 1 μm thick!

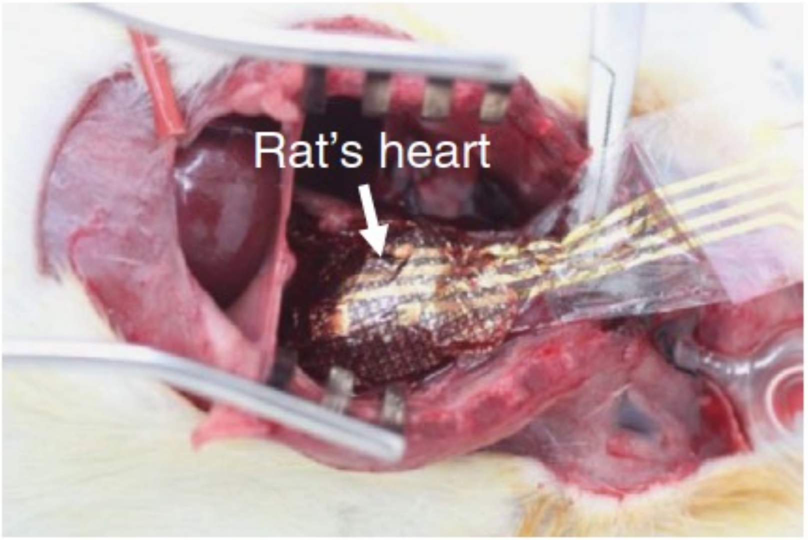


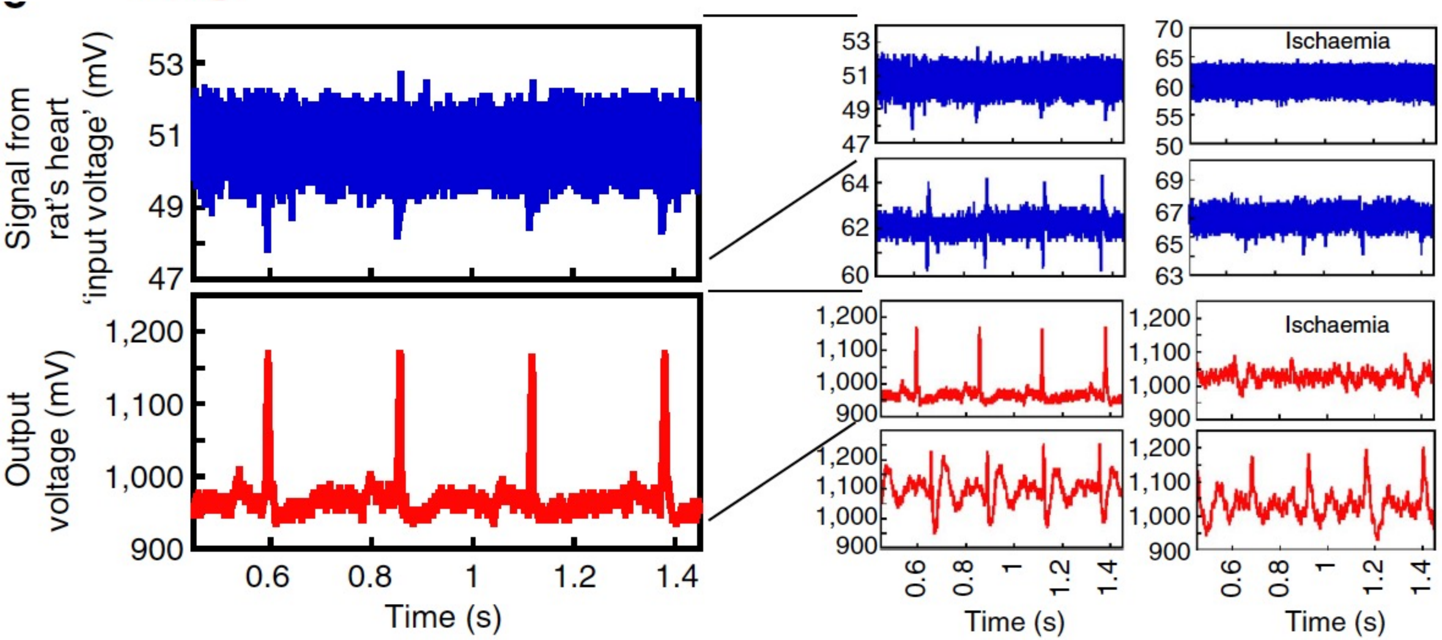


Kaltenbrunner, et al., *Nature*, **499**, 458 (2013).

In Vivo Cardiac Monitoring







Sekitani, et al. *Nat. Comm*. DOI: 10.1038/ncomms11425 (2016)

What we learned

- OTFTs have made extraordinary progress since their first demonstration in 1986
- Their properties can be modified through chemical design
- Morphology is key to high performance
- Very small gate transistors are common in BG/TC configurations
- Very large circuits demonstrated (100's of transistors)
- Reliability depends on exposure to contaminants
- Most promising applications in sensing and medicine
- But….there is no "killer app" yet identified that can drive this technology to a commercial success